

**REMARKS**

Applicant notes the Examiner did not acknowledge receipt of the foreign priority document which Applicant forwarded with the Patent Application on November 13, 2000. Applicant respectfully requests Examiner acknowledge receipt of the foreign priority document.

Applicant has set forth drawing corrections to Figures 4, 5A, and 5B which now include the designation "prior art" as requested by the Examiner. Applicant requests reconsideration of the rejection to the drawings set forth in paragraph 2 of the Examiner's Action regarding the static electricity drawing wire 401 protruding from the fingerprint recognizing surface upwardly. Applicant notes that this is clearly illustrated in Figure 3, wherein the static electricity discharge electrodes 501 extends from the surface of the insulating material 502. Accordingly, Applicant submits that no drawing change is required.

In regard to the objections set forth in paragraph 3, Applicant submits that the amendments set forth herein to the claims overcome these objections. Accordingly, in light of these modifications, Applicant requests the Examiner now withdraw the objections to the claims.

Additionally, in regard to the rejections set forth by the Examiner under 35 U.S.C. § 112, first paragraph, Applicant has modified the claims to clarify the referenced subject matter. Applicant submits that the recitation in the original claims of "said second surface is substantially equivalent to a surface of said insulating film" is clearly illustrated in

Figure 2, wherein the top surface of the second electrode 401 is at a same level as the top surface of the insulating film. Applicant has modified the claims to more clearly express this subject matter. Accordingly, Applicant requests the Examiner now withdrawn the rejections under U.S.C. § 112.

Applicant respectfully requests reconsideration of the prior art rejections set forth by the Examiner under U.S.C. §§ 102 and 103. Applicant respectfully submits that the prior art references of record, whether considered alone or in combination, fail to either teach or suggest Applicant's presently claimed invention. More specifically, Applicant's claimed invention is directed to fingerprint identification system comprised of a semiconductor substrate wherein discharge electrodes are located between the electrodes that are used for measuring the capacitance of the system for fingerprint analysis.

Advantageously, these discharge electrodes improve the performance of the device and prevent static electricity from damaging the device and degrading performance.

As now claimed by Applicant in the instant application, both the capacitance measuring electrodes and the static discharge electrodes are advantageously formed concurrently during a single manufacturing process. This is neither taught nor suggested in the cited references of record.

In order to express these distinctions, Applicant has modified the independent claims to reflect that the bottom level of both the first and second electrodes is the same, which occurs during a single manufacturing process.

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In contrast, the Thomas reference United States Patent No. 6,326,277 merely describes a system wherein the capacitance measuring electrodes are initially formed and thereafter, after subsequent layers are formed, the electrodes for discharging static electricity are formed in a subsequent manufacturing process. Applicant submits that the present invention is patentably distinct over this art because a separate process for formation of adhesive electrodes is not required.

In light of the foregoing, Applicant requests the Examiner now withdraw the claim rejections and allow all claims in the application.

Respectfully submitted,

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FIG. 3

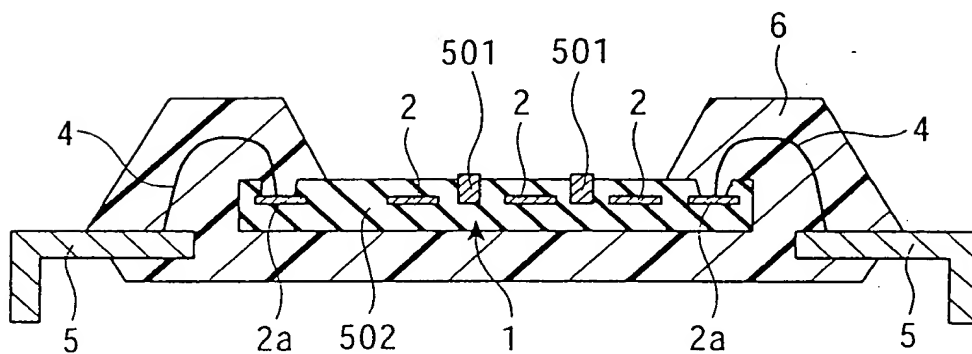
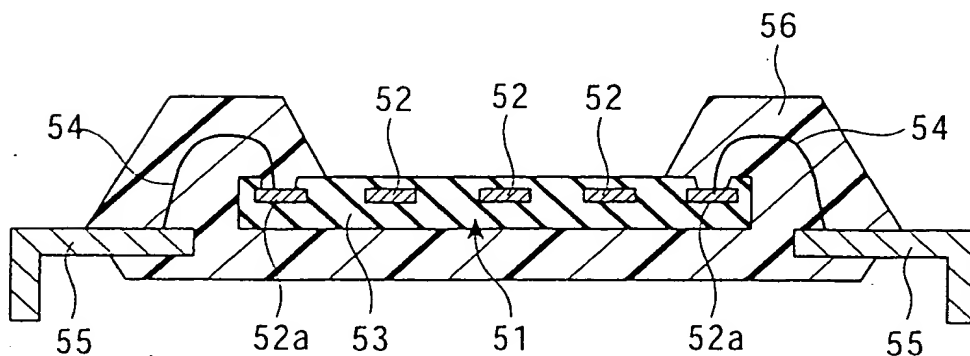
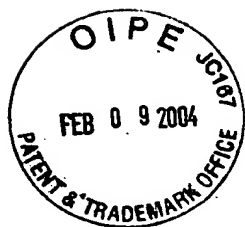


FIG. 4 *PRIOR ART*



 $3/3$ 

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Prior Art

Figure 7 is a cross-sectional view of a semiconductor device. It illustrates two distinct regions, labeled (52, 2) and (53, 3), which are part of a larger substrate 10. Both regions contain a stack of layers: a bottom layer 10, a middle layer 20, and a top layer 21. The distance from the top surface of layer 20 to the uppermost surface 70 is denoted as  $d_1$  for region (52, 2) and  $d_2$  for region (53, 3). An inset at the top right provides a perspective view of a curved surface 7, which is indicated by an arrow pointing to the upper boundary of the device structure.

FIG. 5B

